CBCS SCHEME

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21EC32

Third Semester B.E. Degree Examination, June/July 2024
Digital System Design using Verilog

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. The input to a combinational logic circuit is a valid single digit BCD data. Design the logic circuit using minimum hardware to detect whenever a number greater than 5 appears at the input. **(08 Marks)**

b. Expand $f_1 = a + ab + a\bar{c}\bar{d}$ into minterm and $f_2 = a.(b + c).(a + c + \bar{d})$ into maxterm. **(06 Marks)**

c. Reduce the following function using K-map technique and implement using gates.
$f(P, Q, R, S) = \Sigma m(0, 1, 4, 8, 9, 10) + \Sigma d(2, 11)$ **(06 Marks)**

OR

2 a. Identify all prime implicants and essential prime implicants of the following function using K-map.
$f(a, b, c, d) = \Sigma m(0, 1, 2, 5, 6, 7, 8, 9, 10, 13, 14, 15)$ **(06 Marks)**

b. Simplify the following Boolean function using Quine McCluskey method.
$F(A, B, C, D) = \Sigma m(0, 2, 3, 6, 7, 8, 10, 12, 13)$ **(10 Marks)**

c. Minimize the expression using K-map
$Y = (A+B+\overline{C})\cdot(A+\overline{B}+\overline{C})\cdot(\overline{A}+\overline{B}+\overline{C})\cdot(\overline{A}+B+C)\cdot(A+B+C)$ **(04 Marks)**

Module-2

3 a. Design 2-bit magnitude comparator. **(10 Marks)**

b. Implement $f(w, x, y, z) = \Sigma m(0, 4, 8, 10, 14, 15)$ using
i) 8×1 MUX with w, x, y as select lines.
ii) 4×1 MUX with w, x as select lines. **(06 Marks)**

c. Implement full adder using 74138 decoder. **(04 Marks)**

OR

4 a. Explain the general structure of PLDs. **(06 Marks)**

b. Construct 4 to 16 line decoder from 2 to 4 line decoder and implement the Boolean function.
$f(x_3, x_2, x_1, x_0) = \Sigma m(0, 6, 9, 11, 15)$ **(08 Marks)**

c. Design 3 bit binary full subtractor using logic gates. **(06 Marks)**

Module-3

5 a. With neat diagram explain Master Slave JK Flip Flop. **(08 Marks)**

b. Explain 4 bit universal shift register. **(08 Marks)**

c. Obtain the characteristics equation for SR and T Flip Flop. **(04 Marks)**

OR

6 a. Explain the working of Mod-4 twisted ring counter. **(07 Marks)**

b. Design 4 bit binary ripple counter using T Flip Flop. **(06 Marks)**

c. Design Mod-6 synchronous counter using clocked JK Flip Flop. **(07 Marks)**

Module-4

7 a. With general syntax and suitable examples, explain the shift operators available in verilog. **(06 Marks)**

b. List and explain the verilog data types. **(08 Marks)**

c. Realize full adder circuit using verilog data flow description. **(06 Marks)**

OR

8 a. Write a verilog code for a 2 × 1 multiplexer in dataflow description using signal assignment. **(06 Marks)**

b. List all the different styles of descriptions, explain the structure of dataflow description. **(06 Marks)**

c. Explain the following in data flow description:
i) Signal declaration and assignment statement
ii) Constant declaration and assignment statement
iii) Concurrent signal assignment statement
iv) Assigning a delay time to the signal assignment statement. **(08 Marks)**

Module-5

9 a. Explain CASE statement with syntax. Write a behavioral description of a positive edge triggered JK Flip Flop using CASE statement in verilog. **(10 Marks)**

b. Write verilog behavioral description of 8×1 MUX. **(06 Marks)**

c. Write a verilog program for half adder using structural description. **(04 Marks)**

OR

10 a. With example, explain the syntax of following sequential statements:
i) If ii) Else if **(06 Marks)**

b. List and explain all the loop statements in verilog. **(08 Marks)**

c. Write a verilog program for 3 bit binary counter using case statement. **(06 Marks)**

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